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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,324	01/09/2004	Akira Umezawa	247512US2S	7249

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EXAMINER	
ERDEM, FAZLI	
ART UNIT	**PAPER NUMBER**
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/09/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/753,324	UMEZAWA ET AL.	
	Examiner	Art Unit	
	Fazli Erdem	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8,9,14-16,21,22,27-30 and 35-37* is/are rejected.

7)☒ Claim(s) *4-7, 10-13, 17-20, 23-26 and 31-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Terminal disclaimer for 11/111870 application has been received and accepted on 11/12/2006. However, after further review and search, this action is issued and made non-final.

Allowable Subject Matter

1. Claims 4-7, 10-13, 17-20, 23-26 and 31-34 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior art failed to establish write global bit line and read global bit line and the required third MOS transistors with gates connected to local bit lines sharing the global bit lines independent from each other.

Claim Objections

Regarding Claims 2 and 29, the limitation " the data is written into the plurality of memory cells connected to the same one of the word lines are written into at the same time" is considered indefinite.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 8, 9, 14-16, 21, 22, 27-30 and 35-37 rejected under 35 U.S.C. 102(b) as being anticipated by Onakado et al. (5,818,761).

Regarding Claim 1, Onakado et al. disclose a non-volatile semiconductor memory device capable of high speed programming/erasure where in Fig. 10 it is disclosed a plurality of memory cells each of which include a first MOS transistor 24 with a charge accumulation layer (FG in drawing) and a control gate (CG in drawing) and a second MOS transistor (the figure actually shows 4 separate MOS transistors labeled as 24) which has one end of its current path connected to one end of a current path of the first MOS transistor (also see Fig. 11, M00 through M03 and M10 through M13), plurality of local bit lines/sub bit lines SB01, SB02, SB11, SB12 in Fig. 11 and SBL0-SBL12 in Fig. 39, each of which connects other ends of the current paths of the first MOS transistors, a global bit line/main bit line MB0, MB1 in Fig. 11 and MBL in Fig 39 to which two or more local bit lines/sub bit lines SBL/SB are connected in common, a first switch element SGL1 in Fig. 39 which makes connection between the local bit lines/sub bit lines SBL and the global/main bit line MBL in Fig. 39, a holding/latch circuit 220 in Fig. 39 and 53 in Fig. 11 which is connected to global/main bit line and holds data to be written into the memory cells.

Regarding Claim 2, word lines (WL0-WL3 in Fig. 39 and 11) are connected to control gates of the plurality of the memory cells in common where the data is written into the plurality of memory cells connected to the same one of the word lines and written at the same time.

Regarding Claim 3, FN tunneling is described in Fig. 17, column 29, lines 5-25, column 2, lines 45-57 and in Fig 46 and column 3, lines 30-45 and in Fig. 47.

Regarding Claim 8, in Fig. 17, source line is connected to end of current path of the second MOS transistors MC and a 1.5 V source line driver supplies potential to the source line SL.

Regarding Claim 9, in Figs 4 and 5, a negative voltage is applied to the local bit lines/sub bit lines SBL in a write operation and a negative voltage is applied to the control gate of the first MOS transistor in an erase operation.

Regarding Claim 14, in Figs. 10 and 39, global bit line / main bit line MBL is made of a metal wiring layer located at the highest level in a memory cell array which has the memory cells arranged in a matrix.

Regarding Claim 15, Onakado et al. disclose a non-volatile semiconductor memory device capable of high speed programming/erasure where in Fig. 10 it is disclosed a plurality of memory cells each of which include a first MOS transistor 24 with a charge accumulation layer (FG in drawing) and a control gate (CG in drawing), plurality of local bit lines/sub bit lines SB01, SB02, SB11, SB12 in Fig. 11 and SBL0-SBL12 in Fig. 39, each of which connects other ends of the current paths of the first MOS transistors, a

global bit line/main bit line MB0, MB1 in Fig. 11 and MBL in Fig 39 to which two or more local bit lines/sub bit lines SBL/SB are connected in common, a first switch element SGL1 in Fig. 39 which makes connection between the local bit lines/sub bit lines SBL and the global/main bit line MBL in Fig. 39, a holding/latch circuit 220 in Fig. 39 and 53 in Fig. 11 which is connected to global/main bit line and holds data to be written into the memory cells, word lines (WL0-WL3 in Fig. 39 and 11) are connected to control gates of the plurality of the memory cells in common, the data being written into two or more of the memory cells connected to the same word line at the same time by exchanging electrons with the charge accumulation layer by FN tunneling as described in Fig. 17, column 29, lines 5-25, column 2, lines 45-57 and in Fig 46 and column 3, lines 30-45 and in Fig. 47

Regarding Claim 16, each of the memory cells further includes a second MOS transistor (the figure actually shows 4 separate MOS transistors labeled as 24) which has one end of its current path connected to one end of a current path of the first MOS transistor (also see Fig. 11, M00 through M03 and M10 through M13)

Regarding Claim 21, in Fig. 17, source line is connected to end of current path of the second MOS transistors MC and a 1.5 V source line driver supplies potential to the source line SL.

Regarding Claim 22, in Figs 4 and 5, a negative voltage is applied to the local bit lines/sub bit lines SBL in a write operation and a negative voltage is applied to the control gate of the first MOS transistor in an erase operation.

Regarding Claim 27, in Figs. 10 and 39, global bit line / main bit line MBL is made of a metal wiring layer located at the highest level in a memory cell array which has the memory cells arranged in a matrix.

Regarding Claim 28, Onakado et al. disclose a non-volatile semiconductor memory device capable of high speed programming/erasure where in Fig. 10 it is disclosed a plurality of memory cells each of which include a first MOS transistor 24 with a charge accumulation layer (FG in drawing) and a control gate (CG in drawing) and a second MOS transistor (the figure actually shows 4 separate MOS transistors labeled as 24) which has one end of its current path connected to one end of a current path of the first MOS transistor (also see Fig. 11, M00 through M03 and M10 through M13), plurality of local bit lines/sub bit lines SB01, SB02, SB11, SB12 in Fig. 11 and SBL0-SBL12 in Fig. 39, each of which connects other ends of the current paths of the first MOS transistors, a global bit line/main bit line MB0, MB1 in Fig. 11 and MBL in Fig 39 to which two or more local bit lines/sub bit lines SBL/SB are connected in common, a first switch element SGL1 in Fig. 39 which makes connection between the local bit lines/sub bit lines SBL and the global/main bit line MBL in Fig. 39, a holding/latch circuit 220 in Fig. 39

and 53 in Fig. 11 which is connected to global/main bit line and holds data to be written into the memory cells.

Regarding Claim 29, word lines (WL0-WL3 in Fig. 39 and 11) are connected to control gates of the plurality of the memory cells in common where the data is written into the plurality of memory cells connected to the same one of the word lines and written at the same time.

Regarding Claim 30, FN tunneling is described in Fig. 17, column 29, lines 5-25, column 2, lines 45-57 and in Fig 46 and column 3, lines 30-45 and in Fig. 47.

Regarding Claim 35, in Fig. 17, source line is connected to end of current path of the second MOS transistors MC and a 1.5 V source line driver supplies potential to the source line SL.

Regarding Claim 36, in Figs 4 and 5, a negative voltage is applied to the local bit lines/sub bit lines SBL in a write operation and a negative voltage is applied to the control gate of the first MOS transistor in an erase operation.

Regarding Claim 37, in Figs 4 and 5, a negative voltage is applied to the local bit lines/sub bit lines SBL in a write operation and a negative voltage is applied to the control gate of the first MOS transistor in an erase operation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FE
February 28, 2007

SUE A. PURVIS
SUPERVISORY PATENT EXAMINER